L Number	Hits	Search Text	DB	Time stamp
1	756	(calculating or calculated or calculation) with (polish or polished or polishing)	USPAT; US-PGPUB	2003/07/22 12:34
2	620	((calculating or calculated or calculation) with (polish or polished or polishing)) and @ad<20010831	USPAT; US-PGPUB	2003/07/22 12:34
3	470	(((calculating or calculated or calculation) with (polish or polished or polishing)) and @ad<20010831) and thickness	USPAT; US-PGPUB	2003/07/22 12:35
4	170	((((calculating or calculated or calculation) with (polish or polished or polishing)) and @ad<20010831) and thickness) and (planarization or planarize or planarizing)	USPAT; US-PGPUB	2003/07/22 13:27
5	1	("5695601").PN.	USPAT; US-PGPUB	2003/07/22 13:27

DOCUMENT-IDENTIFIER: US 20020042243 A1

TITLE: Polishing body, polishing apparatus, polishing apparatus adjustment method, polished film thickness or polishing endpoint measurement method, and semiconductor device manufacturing method

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (14):

[0012] Conventionally, the endpoint of CMP **polishing** has been determined by time control using the formula of Preston on the basis of the **polishing** rate **calculated** by means of film thickness measurement using an ellipsometer, etc., after **polishing** several tens of dummy samples and performing a cleaning process. In CMP, however, variation occurs in the polishing rate because of the temperature distribution of the polishing body and local differences in the polishing agent supply conditions. Furthermore, because of variations in the surface conditions of the polishing body, the polishing rate drops with the number of wafers processed, and there are differences in the polishing rate due to individual differences between polishing bodies, etc. Accordingly, it is difficult to determine the endpoint of polishing by performing a specified amount of polishing using time control.

Detail Description Paragraph - DETX (25):

[0123] Accordingly, the above-mentioned time interval can be **calculated** or measured beforehand, and the **polished**-state measuring device 23 can be actuated

after this time interval has elapsed following the output of the trigger signal by the position detection sensor. As a result, it is always possible to detect the polishing endpoint or measure the film thickness at the opening part 32a.

Detail Description Paragraph - DETX (38):

[0135] In the initial state immediately following the initiation of polishing, the part 33a, in which the amount of recess of the surface of the window plate 31 on the side of the object of polishing with respect to the surface of the polishing body is smallest, is used for the observation of the state of the polished surface. As a result, the state of the polished surface is observed using the light that passes through the part 33a of the window plate 31 (among the light that is emitted from the polished-state measuring device 23, reflected by the polished surface of the silicon wafer 17 and returned to the polished-state measuring device 23). A position detection sensor (not shown in the figures) is installed on the platen 20 in the same manner as in the polishing apparatus described in Working Configuration 1-2. The time interval required for the platen 20 to rotate from the position of the platen 20 at which the position detection sensor outputs a trigger signal to the position at which the part 33a of the window plate 31 installed in the opening part reaches a point above the polished-state measuring device 23 is determined by the rpm of the platen 20. Accordingly, as in Example 1-2, the time interval can be **calculated** or measured beforehand, and the **polished**-state measuring device 23 can be actuated after this time interval has elapsed following the output of the trigger signal by the position detection sensor.

Detail Description Paragraph - DETX (49):
[0145] In the initial state immediately following the initiation of polishing, the area of 34a in which the amount of recess of the surface of the window 31 on the side of the object of polishing with respect to the surface of the polishing body is smallest is used for the observation of the state of the polished surface. As a result, the state of the polished surface is observed using the light that passes through the area of 34a on the window plate 31 (among the light that is emitted from the polished-state measuring device 23, reflected by the polished surface of the silicon wafer 17 and returned to the polished-state measuring device 23). A position detection sensor (not shown in the figures) is installed on the platen 20 in the same manner as in the polishing apparatus according to Working Configuration 1-2. The time interval required for the platen 20 to rotate from the position of the platen 20 at which the position detection sensor outputs a trigger signal to the position at which the area of 34a on the window 31 installed in the opening part reaches a point above the polished-state measuring device 23 is determined by the rpm of the platen 20. Accordingly, as in Example 1-2, the above-mentioned time interval can be **calculated** or measured beforehand, and the **polished**-state measuring device 23 can be actuated after this time interval has elapsed following the output of the trigger signal by the position detection sensor.

Detail Description Paragraph - DETX (201):
[0294] In all of the examples described above, it is desirable to use a device that detects the polishing endpoint and measures the film thickness from the reflective spectroscopic characteristics (i.e., the

reflective spectrum) as
the polished-state measuring device 23 that is installed beneath the platen 20.
Calculation of the film thickness or detection of the **polishing** endpoint is
accomplished by comparing the reflective spectrum measured by the
polished-state measuring device 23 with a reference spectrum obtained by
simulation, etc., in a computer (not shown in the figures).
Furthermore, it
would also be possible to use a device that detects the polishing endpoint or
measures the film thickness from variations in the reflectivity at a specified
wavelength, or a device that detects the polishing endpoint or measures the
film thickness by imaging the polished surface with a CCD camera, etc., and
subjecting the image thus acquired to image processing, etc., as the
polished-state measuring device 23 instead of the device that detects the
polishing endpoint and measures the film thickness from the reflective
spectroscopic characteristics (reflective spectrum).

DOCUMENT-IDENTIFIER: US 20020037649 A1

TITLE: Method for carrying out planarization processing

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (24):
[0023] The polishing time is **calculated** by dividing the amount to be removed by the polishing rate.

Summary of Invention Paragraph - BSTX (55):
[0052] For example, a case is considered where the reference point of the polishing pad is disposed at a position "Pa" on the surface to be processed followed by polishing the surface, and then the reference point is shifted to other position "Pb" on the surface to be processed followed by polishing the surface. Depending on the manner in which the reference point of the polishing pad is shifted (for example, when "Pb" is close to "Pa"), wherever the polishing pad is disposed, a certain position "Za" on the surface to be processed is beneath the polishing pad (i.e. a part of the polishing pad exists on the position "Za"). In that case, the position "Za" on the surface to be processed is polished twice. Therefore, the processed amount at the position "Za" on the surface is a sum of a product of "Ma" and "ta", i.e. "Ma.times.ta" and a product of "Mb" and "tb", i.e. "Mb.times.tb" (that is "Ma.times.ta"+"Mb.times.tb"), wherein "Ma" is a polishing rate at the position "Za" on the surface when the polishing pad is disposed at the position "Pa"; "ta" is a residence time of the polishing pad at the position "Pa"; "Mb" is a

polishing rate at the position "Za" on the surface when the polishing pad is disposed at the position "Pb"; and "tb" is a residence time of the polishing pad at the position "Pb." In such a case, in order to make the processed amount at the position "Za" desired, the residence times "ta" and "tb" of the polishing pad are determined by solving simultaneous equations or **calculated** by using matrices, as described later.

Summary of Invention Paragraph - BSTX (59):
[0056] Next, a manner to determine the residence time of the polishing pad at each position so that a distribution of the processed amounts on the surface to be processed is as desired will be explained concretely. The residence time is determined by **calculating** from the desired processed amount at each position on the surface to be processed and a polishing rate which has been measured at each position on the surface to be processed. The manner is explained in detail hereinafter.

Summary of Invention Paragraph - BSTX (76):
[0073] The polishing rate of the workpiece at each position is thus determined under a predetermined condition, and then the residence time of the polishing pad at each position is determined so as to adjust the processed amount of the surface to be processed at each position to a predetermined one. Concretely, in a case where the predetermined amount to be processed at each position is arranged together as a matrix "H", and each residence time of the polishing pad at each position is arranged together as a matrix "T", since the relationship of "H=A.multidot.T" is maintained, the residence times can be determined by **calculating** the product of the inverse matrix A.sup.-1 of the

matrix "A" and the matrix "H".

Summary of Invention Paragraph - BSTX (79):
[0076] **calculating** the product of the inverse matrix "A.sup.-1" of the matrix "A" and the matrix "H" to determine a matrix "T" having (n+1) rows and one column ((n+1).times.1) in which an element located in the (x+1)th row represents as "t.sub.xd" the residence time of the polishing pad at the position where the center of the polishing pad is "xd" apart from the center of the workpiece wherein "x" is an integer of 0 to n.

Detail Description Paragraph - DETX (20):
[0110] The sort of the polishing pad, the area of the polishing pad, the conditions of the oscillation of the polishing pad, and the sort of the polishing slurry, and if necessary, the conditions of the rotational motion of the polishing pad are thus determined according to the surface to be processed of the workpiece, and further, the pressure which is exerted between the polishing pad and the surface to be processed, the rotating speed of the workpiece, and the shift length "d" per time of the polishing pad are suitably established, and then the residence time of the polishing pad at each position is determined. Concretely, as mentioned above, the residence time at each position is determined as a matrix "T" which is **calculated from the polishing** rate (the matrix "A") at each position under the predetermined conditions and the predetermined amount (the matrix "H") to be processed at each position.

Claims Text - CLTX (7):
6. The method for carrying out a planarization processing according to claim 5, wherein when the center of said disc-shaped

polishing pad is shifted
"n" times (wherein "n" is an integer of 1 or more) by length "d" in the radial
direction of said disc-shaped workpiece from the center to the periphery of
said disc-shaped workpiece and the residence time of said polishing pad at each
position is determined by: previously determining a (n+1).times.(n+1) matrix
"A" of which an element "a.sub.ydxd" located in the (y+1)th row and the (x+1)th
column represents a polishing rate of said surface to be processed at the
position which is "yd" apart from the center of said workpiece when said
polishing pad is disposed at a position where the distance between the center
of said polishing pad and the center of said workpiece is "xd", wherein "x" is
an integer of 0 to n; arranging the desired processed amounts of said
workpiece in a (n+1).times.1 matrix "H" in which an element located in the
(y+1)th row represents as "h.sub.yd" the desired processed amount at the
position which is "yd" apart from the center of said workpiece wherein "y" is
an integer of 0 to n; **calculating** the product of the inverse matrix "A.sup.-1"
of the matrix "A" and the matrix "H" to determine a (n+1).times.1 matrix "T" in
which an element located in the (x+1)th row represents as "t.sub.xd" the
residence time of said polishing pad at the position where the center of said
polishing pad is "xd" apart from the center of said workpiece wherein "x" is an
integer of 0 to n.

DOCUMENT-IDENTIFIER: US 20010012108 A1

TITLE: METHODS AND APPARATUS FOR THE IN-PROCESS MEASUREMENT OF THIN FILM LAYERS

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (9):

[0008] Presently known methods for measuring the thickness of an oxide layer on a semiconductor wafer involve measuring the total thickness of an applied oxide layer, determining the desired thickness of the oxide layer after **planarization, calculating** the pressure to be applied during the polishing or planarization process, and further **calculating** the approximate time required to remove a predetermined amount of oxide layer for a given pressure and slurry combination. Once the desired removal rate (often expressed in nanometers per minute) is ascertained, a statistical inference is employed to determine the approximate amount of time necessary to remove a desired amount of material. After the wafers have undergone planarization for an amount of time calculated to remove a desired thickness of the oxide layer, the workpieces are removed from the machine and the actual thickness of the oxide layer is measured, for example, through the use of laser interferometric techniques. If it is determined that the oxide layer is still too thick after initial planarization, the workpieces must be reinstalled onto the CMP machine for further oxide layer removal. If, on the other hand, an excessive amount of oxide layer has been removed, it may be necessary to scrap the disks, resulting in substantial

unnecessary costs.

US-PAT-NO: 6530822

DOCUMENT-IDENTIFIER: US 6530822 B1

TITLE: Method for controlling polishing time in chemical-mechanical polishing process

---------- KWIC ---------

Brief Summary Text - BSTX (8):

where removal thickness and polishing rate are constants. Accordingly the **calculated polishing** time is surely a constant. That is, every lot of the production wafers is put into the CMP apparatus and is polished for the same period of time due to the same values of removal thickness and polishing rate. The variability of the original thickness of oxide layers is not considered during the chemical-mechanical polishing process. The polishing rate is generally found from the periodic machine tests, in which the dummy wafer is employed. Then, every lot of production wafers sent into the polishing machine is polished under the set of the constant polishing rate for the rough constant polishing time. However, in the repetitionary chemical-mechanical polishing processes, the polishing rate is easily changed for reasons including the impact of some elements such as pads and dressers in the integrated circuits, and consuming of the polishing pad of the machine. In conventional procedures, to get an accurate polishing time, a greater number of machine tests should be done, and the production processes should certainly be paused more frequently. After that, unfortunately, the throughput will be reduced and the cost of

ownership will be increased.

Detailed Description Text - DETX (9):

where T_1 is the polishing time for the first lot of production wafers in the chemical-mechanical polishing step. When the polishing step is completed, the first lot of production wafers is moved into a post-CMP metrology 13 to measure the thickness of the polishing-desired layer of each wafer, which is the so-called post-thickness TK_{A1}. Then the real polishing rate RR_1 for the chemical-mechanical polishing step can be **calculated** through the CMP semi-automated system 14. When the chemical-mechanical polishing goes on being implemented lot by lot, the polishing ability of the polishing pads set in the CMP apparatus will be reduced little by little due to consumption. Additionally, the impact of some elements such as pads or dressers in the integrated circuits substantially reduces the polishing rate too. That is, the polishing rate will not always be constant when the production wafers are polished lot by lot, even though they have the same structure and materials thereon. If the chemical-mechanical polishing step is implemented through the polishing rate of RR_0 until the thickness of the polishing-desired layer of the wafers is TK_{Target}, the desired polishing time is T. Accordingly, we can find the removal thickness $RR_0 *T$. On the other hand, if the chemical-mechanical polishing step is implemented through the polishing rate of RR_1 for the same polishing time T, we can get the removal thickness $RR_1 *T$. After being polished, the thickness of the polishing-desired layer is changed to TK_{A1}. The relationship can be expressed by:

US-PAT-NO: 6489624

DOCUMENT-IDENTIFIER: US 6489624 B1

TITLE: Apparatus and methods for detecting thickness of a patterned layer

---------- KWIC ---------

Brief Summary Text - BSTX (11):

In the interference techniques, changes in an interference pattern in reflected light are monitored over time. I.e., the interference pattern changes as the thickness of the subject layer changes. The layer thickness or amount of polishing of the subject layer that has occurred can be **calculated** from such data.

Brief Summary Text - BSTX (32):

Generally speaking, in determining a "polishing endpoint" (i.e., a desired thickness of the subject layer at which polishing should stop), the spectral reflectance or spectral transmittance curves typically include features that differ significantly from the spectral reflectance or spectral transmittance curves, respectively, produced before reaching the polishing endpoint. Thus, by measuring and/or **calculating** data pertaining to such features, the polishing endpoint can be detected accurately.

Detailed Description Text - DETX (14):

When a subject wafer is multilayered and has a complex structure, it can be difficult to perform calculations of the layer thickness from the spectral

characteristics of reflected signal light. In such an instance, it is effective to calculate the spectral reflected waveform in advance (this is easier than performing a reverse **calculation** from the waveform itself) from data concerning the wafer structure and the specific layer thickness desired when the polishing endpoint is reached. In determining the polishing endpoint, the shape of the waveform **calculated** in advance is compared to the shape of a measured waveform. (Typically, the maxima and minima observed in the calculated waveform are at the same wavelengths as maxima and minima in the measured waveform.)

Detailed Description Text - DETX (87):

In this working example, similar measurements were performed as in Working Example 1. The spectral characteristics of the reflected probe light (i.e., signal light) at the polishing endpoint were **calculated** in advance. Comparisons were made of the calculated and measured minima and maxima in the spectral distribution. Whereas the absolute value of the spectral distribution did not match that of the calculated reflected-light spectral distribution, there was an excellent match of the locations of the minima and maxima of each spectrum. By using such a basis for determining polishing endpoint (i.e., using **calculated** minima and maxima), polishing endpoints were determined with a film-thickness precision of about 10 percent.

US-PAT-NO: 6484300

DOCUMENT-IDENTIFIER: US 6484300 B1

TITLE: Systems, methods and computer program products for obtaining an effective pattern density of a layer in an integrated circuit, and for simulating a chemical-mechanical polishing process using the same

---------- KWIC ---------

Detailed Description Text - DETX (38):
In embodiments that use an equation to calculate the variation of each parameter, the relative velocity of the wafer with respect to the polishing pad, and the downward polishing pressure of a wafer on the polishing pad, which can vary according to the position of each pattern cell within the wafer, may be considered as the most variable parameters. In detail, the relative velocity of the wafer with respect to the polishing pad may be **calculated** by:
##EQU7##

Detailed Description Text - DETX (55):
CMP simulation according to embodiments of the present invention may be embodied in a general purpose digital computer by running a program from a computer usable medium, including but not limited to storage media such as magnetic storage media (e.g., ROM's, floppy disks, hard disks, etc.), optically readable media (e.g., CD-ROMs, DVDs, etc.) and carrier waves (e.g., transmissions over the Internet). Hence, the present

invention may be embodied
as a computer usable medium having a computer readable program embodied therein
for CMP simulation, the computer readable program in the computer usable medium
comprising: computer readable program code that causes a computer to effect
defining pattern cells with respect to layout data of a predetermined material
layer pattern; computer readable program code that causes a computer to effect
computing the pattern density with respect to each pattern cell; computer
readable program code that causes a computer to effect **calculating** the pattern
density with respect to each pattern cell, in consideration of the effects of
the patterns of each of the peripheral pattern cells of a selected pattern cell
on the pattern density of the selected pattern cell, for each of the pattern
cells; and computer readable program code that causes a computer to effect
computing the thickness and the step difference distribution of a planarization
layer stacked on the material layer with polishing time, using the effective
pattern density of each pattern cell, for instance. A functional program, code
and code segments, used to implement each program module of the present
invention, can be derived by a skilled computer programmer from the description
of the invention contained herein.

Claims Text - CLTX (7):

7. A method according to claim 1 wherein the layer is a patterned layer
upon which a planarization layer is formed and planarized using
Chemical-Mechanical Polishing (CMP), and wherein the **calculating** step is
followed by: determining a thickness of the planarization layer as a function
of CMP polishing time, based on the effective pattern density.

Claims Text - CLTX (14):
12. A method according to claim 1 wherein the following step is performed after the step of **calculating**: determining a stop time for chemical mechanical polishing a layer on the patterned layer, based upon the effective pattern density.

Claims Text - CLTX (15):
13. A method according to claim 1 wherein the following step is performed after the step of **calculating**: determining monitoring points for chemical mechanical polishing a layer on the patterned layer, based upon the effective pattern density.

Claims Text - CLTX (16):
14. A method according to claim 1 wherein the following steps are performed after the step of **calculating**: determining a portion of a layer on the patterned layer that will thin during chemical mechanical polishing the layer, based upon the effective pattern density; adding a dummy pattern to a corresponding portion of the patterned layer; and wherein the defining step is responsive to the layout data and to the dummy pattern.

Claims Text - CLTX (23):
21. A system according to claim 15 wherein the layer is a patterned layer upon which a planarization layer is formed and planarized using Chemical-Mechanical Polishing (CMP), the system further comprising: means for determining a thickness of the planarization layer as a function of CMP polishing time, based on the effective pattern density, in response to the means for **calculating**.

US-PAT-NO: 6466642

DOCUMENT-IDENTIFIER: US 6466642 B1

TITLE: Methods and apparatus for the in-situ measurement of CMP process endpoint

---------- KWIC ---------

Brief Summary Text - BSTX (8):
Presently known methods for measuring the thickness of a material layer on a semiconductor wafer involve measuring the total thickness of an applied material layer, determining the desired thickness of the material layer after **planarization, calculating** the pressure to be applied during the polishing or planarization process, and further **calculating** the approximate time required to remove a predetermined amount of material layer for a given pressure and slurry combination. Once the desired removal rate (often expressed in nanometers per minute) is ascertained, a statistical inference is employed to determine the approximate amount of time necessary to remove a desired amount of material. After the wafers have undergone planarization for an amount of time calculated to remove a desired thickness of the material layer, the wafers or workpieces are removed from the machine and the actual thickness of the material layer is measured off-line, for example, through the use of laser interferometric techniques. If it is determined that the material layer is still too thick after initial planarization, the workpieces must be reinstalled onto the CMP machine for further material layer removal. If, on the other hand, an

excessive amount of material layer has been removed, it may
be necessary to
scrap the wafers, resulting in substantial unnecessary
costs.

US-PAT-NO: 6439964

DOCUMENT-IDENTIFIER: US 6439964 B1

TITLE: Method of controlling a polishing machine

---------- KWIC ---------

Abstract Text - ABTX (1):

Recipes for the polishing machine, such as recipes for carrier head pressure, are generated from empirical data, and consequently can provide a more accurate prediction than techniques based upon theoretical models. A plurality of test substrates are polished with a plurality of parameter sets. A polishing profile is measured for each of the plurality of test substrates, and a polishing time is **calculated for each polishing** parameter set which minimizes the difference between a predicted substrate profile and a desired substrate profile.

Brief Summary Text - BSTX (8):

In general, in one aspect, the invention is directed to a method of determining a polishing recipe. In the method, a plurality of test substrates are polished with a plurality of parameter sets. A polishing profile is measured for each of the plurality of test substrates, and a polishing time is **calculated for each polishing** parameter set which minimizes the difference between a predicted substrate profile and a desired substrate profile.

Brief Summary Text - BSTX (9):

Implementations of the invention may include one or more of the following.
A device substrate may be polishing using each of the polishing parameter sets in series for the polishing time **calculated** for that parameter set. An initial profile for the device substrate may be determined, and the predicted substrate profile may be **calculated** from a difference between a total polishing profile and the initial polishing profile. The total polishing profile may be **calculated** from a sum of the products of the polishing times and the associated measured profiles of the test substrates.

Brief Summary Text - BSTX (10):
In another aspect, the invention is directed to a method of determining a polishing recipe. In the method, a plurality of test substrates are polished with a plurality of carrier head parameter sets that can be used during polishing of actual device substrates. This includes polishing a first set of test substrates to determine a variation in polishing profile as a function of the contact region diameter and polishing a second set of test substrates to determine the variation in the polishing profile as a function of the retaining ring pressure. An amount of material removed is measured at a plurality of different radial positions on each test substrate, a desired profile is created which represents the desired thickness across the substrate; and a polishing time is **calculated** for each of the plurality of carrier head parameter sets that will result in predicted substrate profile substantially equal to the desired substrate profile.

Detailed Description Text - DETX (3):
In general, the invention provides a method of determining a polishing

recipe to achieve uniform planarity across a wafer surface as a result of chemical mechanical polishing. The method includes polishing a plurality of test substrates with a plurality of test substrates, measuring a polishing profile for each of the plurality of test substrates, and **calculating a polishing** time for each polishing parameter set which minimizes the difference between a predicted substrate profile and a desired substrate profile.

Detailed Description Text - DETX (4):
By performing the method, polishing recipes can be generated automatically. Initially, empirical data is accumulated by measuring the removal profile for each polishing step. In order to generate the polishing recipe, the system calculates a scale factor for each basic polishing step. This scale factor determines the amount of time spent polishing with that parameter profile. The scale factors are selected so that variations in the final wafer profile are minimized. During polishing, each polishing step is performed in series for the **calculated** amount of time.

Detailed Description Text - DETX (9):
Referring to FIG. 3, a recipe for controlling the pressures in the various chambers is generated in a method 200. In general, the polishing method assumes that each step in a series of basic polishing steps (each with a preselected set of carrier head parameters) will be performed. Initially, empirical data is accumulated by measuring the removal profile for each polishing step. In order to generate the polishing recipe, the system calculates a scale factor for each basic polishing step. This scale factor determines the amount of time spent polishing with that

parameter profile. The
scale factors are selected so that variations in the final wafer profile are
minimized. During polishing, each polishing step is performed in series for
the **calculated** amount of time.

Detailed Description Text - DETX (12):
Once the wafers have been polished, the amount of material removed is
measured at several different radial positions on each wafer (step 208). This
creates a "database" with a polishing profile for each set of polishing
parameters. Sample wafer polishing profiles resulting from steps 202-206 are
illustrated in FIG. 3. This database will be used by the recipe generator when
calculating the polishing time for each polishing step.

Detailed Description Text - DETX (17):
where [P.sub.R].sub.i is the removal rate for step i, T.sub.i is polishing
time for step i (to be **calculated** below), T.sub.base is the polishing time for
the test wafers, e.g., 30 seconds, and N is the total number of polishing
steps. The predicted wafer profile [P.sub.P] is simply the difference between
the initial profile and the total removal profile, i.e., [P.sub.P]=[P.sub.I
]-[P.sub.R].sub.T.

Detailed Description Text - DETX (18):
In order to generate the recipe, the recipe generator calculates the set of
polishing times Ti that will result in the minimum variation of the predicted
wafer profile [P.sub.P] from the desired profile [P.sub.D] (step 218). The
minimization can be performed for a certain diameter range across the wafer,
e.g., from 3 to 197 mm, or from 10 to 190 mm, and the like. The minimization
calculation can be performed with conventional techniques.

For example, the matrices [P.sub.D], [P.sub.I], [P.sub.R].sub.i, and the polish times T.sub.i can be entered into cells in an Excel.sup.R spreadsheet, equations equivalent to those set forth above can be entered into the spreadsheet, and the polish times T.sub.i may be **calculated** using the Solver function of Excel to minimize the total difference between the predicted wafer profile [P.sub.P] and the desired profile [P.sub.D]. Alternatively, the polishing times may be optimized also by introducing one or more deviation variables, for example, [z.sub.min] and [z.sub.max] and using them as boundaries to minimize weighted deviations between the predicted wafer profile [P.sub.P] and the desired profile [P.sub.D].

Detailed Description Text - DETX (19):

These **calculated polishing** times T.sub.i can then be entered manually into the chemical mechanical polishing control system, which performs each polishing step in order for the **calculated** amount of time T.sub.i (step 220).

Detailed Description Text - DETX (20):

In a production system, data would be passed automatically between various components. For example, the initial wafer profile would be passed automatically from the metrology system to the recipe generator, and the polishing times Ti would be passed automatically from the recipe generator to the control system. In fact, the recipe generator could be implemented as part of the control system itself. Alternatively, the **calculated polishing** times could be stored as part of a polishing recipe in a separate file in a computer readable medium. The polishing recipe, with the associated polishing times,

could then be loaded into the control software for the polishing apparatus when needed.

Claims Text - CLTX (1):

1. A method of determining a polishing recipe, comprising: polishing a plurality of test substrates with a plurality of polishing parameter sets, the polishing step including polishing at least one test substrate for each polishing parameter set in the plurality of polishing parameter sets; measuring a polishing profile for each of the plurality of test substrates; and **calculating a polishing** time for each polishing parameter set and **calculating,** based on the polishing profiles for the test substrates and the polishing time for each parameter set, a predicted substrate profile that results from polishing a device substrate using each of the plurality of polishing parameter sets for the polish time associated with that polishing parameter set so that the difference between the predicted substrate profile and a desired substrate profile is minimized.

Claims Text - CLTX (2):

2. The method of claim 1, further comprising polishing a device substrate using each of the polishing parameter sets in series for the polishing time **calculated for that polishing** parameter set.

Claims Text - CLTX (4):

4. The method of claim 3, wherein the **calculating** step includes **calculating** the predicted substrate profile from a difference between a total polishing profile and an initial polishing profile.

Claims Text - CLTX (5):

5. The method of claim 4, further comprising **calculating** the total polishing profile from a sum of the products of the polishing times and an associated measured profiles of the test substrates.

Claims Text - CLTX (6):

6. The method of claim 1, wherein **calculating a polishing** time T.sub.i for each polishing parameter set includes representing a total removal profile [P.sub.R].sub.T as ##EQU2##

Claims Text - CLTX (8):

7. The method of claim 6, further comprising iteratively **calculating** T.sub.i to minimize the value of [P.sub.D]-([P.sub.I]-[P.sub.R].sub.T), where [P.sub.D] is a desired polishing profile and [P.sub.I] is a thickness profile of the substrate prior to polishing.

Claims Text - CLTX (11):

10. A method of determining a polishing recipe, comprising: polishing a plurality of test substrates with a plurality of carrier head parameter sets that can be used during polishing of actual device substrates, including polishing a first set of test substrates to determine a variation in polishing profile as a function of a contact region diameter, polishing a second set of test substrates to determine the variation in the polishing profile as a function of a retaining ring pressure; measuring an amount of material removed at a plurality of different radial positions on each test substrate; creating a desired profile which represents a desired thickness across the substrate; and **calculating a polishing** time for each of the plurality of carrier head parameter sets that will result in predicted substrate profile substantially

equal to the desired substrate profile.

US-PAT-NO: 6350393

DOCUMENT-IDENTIFIER: US 6350393 B1

TITLE: Use of CsOH in a dielectric CMP slurry

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Detailed Description Text - DETX (30):

Field measurements were taken from two areas of each wafer--the open field and the array field--and the measurements were used in the efficiency calculations. Array field measurements were taken in close proximity to the stack area. Because wide open (or sparse) areas are typically more problematic in real polishing we also evaluated slurry polishing efficiency by measuring the field in the largest open field area or the 8% area and **calculating** the open field efficiency from the measurement.

Detailed Description Text - DETX (33):

A plot was created for each slurry showing step height vs. time. The curve is fit to the data by interpolating the data along the fitted polishing curve to determine the time at which 95% planarization is achieved (i.e. step height is reduced to 450 .ANG.). Planarization efficiency (.epsilon..sub.p) is **calculated at each of the polishing** intervals using the following formula:
##EQU1##

Detailed Description Text - DETX (38):

Open field and array field efficiencies are dependent upon polishing parameters, polishing machine, and other consumables and

slurries. For
purposes of this application, the term "open field efficiency" and "array field efficiency" refer to the polishing efficiencies determined using an IPEC 472 polishing machine operating at the polishing parameters described above and **calculated** as described above.

US-PAT-NO: 6213844

DOCUMENT-IDENTIFIER: US 6213844 B1

TITLE: Method for obtaining a desired film thickness using chemical mechanical polishing

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Brief Summary Text - BSTX (9):

The amount of material removed during or left remaining after the polishing process is typically controlled by, among other things, running the polishing process for a predetermined amount of time. The amount of time may be adjusted from run to run based on material removal rates from one or more previous polishing runs, wherein the removal rates are **calculated** by measuring the film thickness prior to polishing the wafer and measuring the remaining film thickness after the completion of the polishing process. The film thickness is generally measured using a device such as an x-ray fluorescence machine that is separate from the polishing apparatus. Consequently, the film thickness is typically measured before the wafer is placed on the polishing apparatus and again once the wafer is removed from the apparatus.

Detailed Description Text - DETX (12):

In accordance with an exemplary embodiment of the present invention, film 430 thickness is measured while wafer 125 is coupled to carrier 170. Unlike prior art methods of detecting film 430 endpoint (desired thickness) that continuously measures the film thickness with each oscillation of wafer 125

past the perimeter of pad 250, the methods according to the present invention
include polishing wafer 125 for a predetermined amount of time, measuring the
film thickness at the end of the amount of time, **calculating** an amount of time
to continue polishing, and, if necessary, **polishing for the calculated** amount
of time.

Claims Text - CLTX (17):

8. The method according to claim 7, further comprising the step of
calculating process conditions for a subsequent polish step.

US-PAT-NO: 6207533

DOCUMENT-IDENTIFIER: US 6207533 B1

TITLE: Method for forming an integrated circuit

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Abstract Text - ABTX (1):

In one embodiment, a first dielectric layer (16) is formed overlying a semiconductor substrate (4). A portion of the first dielectric layer (16) is then etched using a patterned masking layer (18). The patterned masking layer (18) is removed and an intermediate polishing layer (20) is formed overlying the first dielectric layer (16). A second dielectric layer (22) is formed overlying the intermediate polishing layer (20), and the second dielectric layer (22) is polished to expose a portion of the intermediate polishing layer (20), and to determine a polishing rate for the second dielectric layer (22). The polishing rate for the second dielectric layer (22) is then used to calculate a polishing time for the first dielectric layer (16), and the first dielectric layer (16) is **polished for the calculated** time.

Detailed Description Text - DETX (9):

The **calculated polishing** rate for dielectric layer 22 is then used to determine at least one polishing condition which is subsequently used to polish dielectric layer 16. In one embodiment, the **calculated polishing** rate for dielectric layer 22 is used to determine a polishing time for dielectric layer 16. In an alternative embodiment, the polishing rate of

dielectric layer 22 is
used as feedback to adjust a polishing condition that changes the subsequent
polishing rate of dielectric layer 16. For example, it may be used to
determine whether or not the surface of the polishing pad needs to be
conditioned prior to polishing dielectric layer 16, or it may be used to adjust
the slurry flow rate, the angular speed of the carrier and the semiconductor
substrate, the angular speed of the polishing pad, the polishing down force
applied to the semiconductor substrate, or the like, when dielectric layer 16
is polished.

Detailed Description Text - DETX (10):
In FIG. 7, dielectric layer 16 is then polished using the previously
determined polishing condition. In one embodiment dielectric layer 16 is
polished, using a polishing time that was **calculated from the polishing** rate of
dielectric layer 22, to expose a portion of patterned trench mask 12, as shown
in FIG. 7. It should be appreciated that the remaining portion of intermediate
polishing layer 20 may be removed either prior to polishing dielectric layer
16, or at the same time that dielectric layer 16 is polished. For example, if
intermediate polishing layer 20 is made of a material which polishes faster
than dielectric layer 16, then it is preferably polished with dielectric layer
16 and removed. However, if intermediate polishing layer 20 polishes at a
slower rate than dielectric layer 16, then it is preferably removed prior to
polishing dielectric layer 16.

US-PAT-NO: 6066266

DOCUMENT-IDENTIFIER: US 6066266 A

TITLE: In-situ chemical-mechanical polishing slurry formulation for compensation of polish pad degradation

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Detailed Description Text - DETX (6):

The film removal rates, **calculated** as described above, of the various layers of a film stack on a particular substrate is then correlated to the order in which the substrate was polished. In other words, the film removal rates of the various layers for the first substrate polished are correlated to substrate number one, the film removal rates of the same layers for the second substrate are correlated to substrate number two and so on until the film removal rates of all the substrates in the substrate lots are determined. At the end of this step, sufficient data to generate a graph (like the one shown in FIG. 1) of film removal rate versus the polishing pad life may be compiled. It is important to note that if the same number of substrate lots that would be polished during a typical CMP cycle are not polished on the test polishing pad to generate a graph like FIG. 1, then extrapolation techniques well known to those skilled in the art may be employed to estimate the actual film removal rate.

US-PAT-NO: 6024628

DOCUMENT-IDENTIFIER: US 6024628 A

TITLE: Method of determining real time removal rate for polishing

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Detailed Description Text - DETX (9):

In FIG. 4, an I-t curve and an I-Dt transformation curve for polishing a patterned material layer is shown. As shown in the figure, since the pattern density is varied during the polishing, the period T is not a constant between every two adjacent peaks. The variation of the period T reflects the variation of the surface pattern density. Therefore, the removal rate for each polishing period T can be **calculated** by substituting the different values of T into Eq. (2).